CLEAN COPY OF AMENDED CLAIMS

sub G8

19. A microprocessor chip, comprising:

instruction pipeline circuitry; and

interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process in accordance with synchronous interrupt criteria, the interrupt criteria being based at least in part on a memory state of the computer and the address of the instruction, wherein the architectural definition of the instruction in an emulated architecture does not call for an interrupt.

sub G13

58. The microprocessor chip of claim 19, wherein the interrupt criteria are further based on the value of the instruction.